

**IN THE UNITED STATES DISTRICT COURT
FOR THE WESTERN DISTRICT OF TEXAS
WACO DIVISION**

ACQIS LLC,
Plaintiff

-v-

MITAC COMPUTING
TECHNOLOGY CORPORATION,
Defendant

6-20-CV-00962

ACQIS LLC,
Plaintiff

-v-

INVENTEC CORPORATION,
Defendant

6-20-CV-00965

ACQIS LLC,
Plaintiff

-v-

ASUSTEK COMPUTER, INC.,
Defendant

6-20-CV-00966

ACQIS LLC,
Plaintiff

-v-

LENOVO GROUP LTD., LENOVO PC
HK LIMITED, LCFC (HEFEI)
ELECTRONICS TECHNOLOGY CO.,
LTD., LENOVO INTERNATIONAL
INFORMATION PRODUCTS
(SHENZHEN) CO. LTD., LENOVO
CENTRO TECNOLÓGICO S DE
R.L. DE CV A MEXICO
CORPORATION, LENOVO
INFORMATION PRODUCTS
(SHENZHEN) CO., LTD.
Defendants

6-20-CV-00967

ACQIS LLC,

Plaintiff

6-20-CV-00968

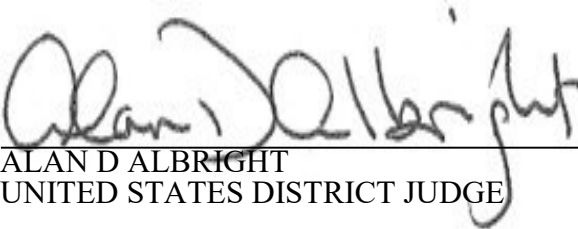
-v-

WIWYNN CORPORATION,
Defendant

CLAIM CONSTRUCTION ORDER

The Court held a *Markman* hearing on November 17, 2021. During that hearing, the Court provided its final constructions. The Court now enters those claim constructions.

SIGNED this 17th day of November, 2021.



ALAN D ALBRIGHT
UNITED STATES DISTRICT JUDGE

Term	Plaintiff's Proposed Construction	Defendants' Proposed Construction	Court's Final Construction
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<p>#1: “Peripheral Component Interconnect (PCI) bus transaction” / ”PCI bus transaction” (proposed by Plaintiff and Defendants)</p> <p>U.S Patent No. 7,676,624, Claims 6, 11</p> <p>U.S. Patent No. 8,041,873, Claims 54, 77, 97</p> <p>U.S. Patent No. 9,529,768 Claims 1, 3-18, 21-22, 30, 33-35, 39-40</p> <p>U.S. Patent No. 9,703,750, Claims 1-2, 4-7, 10-12, 18-21, 25-27, 29, 31, 34-35, 37-38, 44-47</p> <p>U.S. Patent No. 8,626,977, Claims 1, 4, 9-10, 16</p> <p>U.S. Patent No. 8,977,797, Claims 7-8, 10, 14, 16, 36, 38</p> <p>U.S. Patent No. RE45,140, Claims 30-31</p> <p>U.S. Patent No. 8,756,359, Claims 3, 7, 17</p> <p>U.S. Patent No. RE44,739, Claims 29-32</p> <p>U.S. Patent No. RE44,654, Claims 14-16</p> <p>U.S. Patent No. RE43,602, Claim 14</p>	<p>Information, including at least PCI address, data, byte enable, and command type information, in accordance with the industry standard PCI Local Bus Specification, for communication with an interconnected peripheral component</p>	<p>A transaction, in accordance with the industry standard PCI Local Bus Specification, for communication with an interconnected peripheral component</p>	<p>A transaction, in accordance or backwards compatible with the industry standard PCI Local Bus Specification, for communication with an interconnected peripheral component</p>
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U.S. Patent No. RE44,468, Claims 14, 21, 26, 29, 35, 37, 45 U.S. Patent No. RE46,947, Claims 19, 35, 48, 51, 54, 57 U.S. Patent No. RE42,984, Claim 52			
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<p>#2: “address and data bits of a Peripheral Component Interconnect (PCI) bus transaction”/“address and data bits of a PCI bus transaction”/“address bits, data bits, and byte enable information bits of a Peripheral Component Interconnect (PCI) bus transaction”/“address bits, data bits, and byte enable information bits of a PCI bus transaction” (proposed by Plaintiff)</p> <p>Claims reciting specific “bits” of a PCI bus transaction, including but not limited to “address bits,” “data bits,” and “byte enabled information bits” (proposed by Defendants)</p> <p>U.S. Patent No. 9,529,768 Claims 1, 3-18, 21-22, 30, 33-35, 39-40</p> <p>U.S. Patent No. 9,703,750, Claims 1-2, 4-7, 10-12, 18-21, 25-27, 29, 31, 34-35, 37-38, 44-47</p> <p>U.S. Patent No. 8,626,977, Claims 1, 4, 9-10, 16</p> <p>U.S. Patent No. 8,977,797, Claims 7-8, 10, 14, 16, 36, 38</p>	<p>No construction needed.</p> <p>These phrases recite the bits of a PCI bus transaction that are conveyed / transmitted / communicated, <i>i.e.</i>, “address bits,” “data bits,” and “byte enable information bits,” as applicable. Claims that recite these bits do not require that other, non-recited bits be conveyed / transmitted / communicated. The claims, as written, are clear, and this language of the claims does not require construction.</p>	<p>A PCI bus transaction, including all address, data, and control bits</p>	<p>Plain-and-ordinary meaning</p>
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U.S. Patent No. RE45,140, Claims 30-31 U.S. Patent No. 8,756,359, Claims 3, 7, 17 U.S. Patent No. RE44,739, Claims 29-32 U.S. Patent No. RE44,654, Claims 14-16 U.S. Patent No. RE43,602, Claim 14 U.S. Patent No. RE44,468, Claims 14, 26, 29, 35, 37, 45 U.S. Patent No. RE46,947, Claims 19, 35, 48, 51, 54, 57			
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<p>#3: “encoded...” (proposed by Plaintiff) Claims reciting a “encoded” PCI bus transaction or PCI bus transaction in “serial stream” or “serial form” (proposed by Defendants)</p> <p>U.S. Patent No. 9,529,768 Claims 1, 4-10, 13, 15, 18, 21-22, 30, 33-35, 39-40 U.S. Patent No. 9,703,750, Claims 1, 5-7, 10-12, 14, 18-21, 25, 27, 29, 31, 35, 37-38, 44-47 U.S. Patent No. 8,626,977, Claims 1, 4, 6, 9-10, 16 U.S. Patent No. 8,977,797, Claims 7-8, 10, 14, 16, 36, 38 U.S. Patent No. RE45,140, Claims 30-31 U.S. Patent No. 8,756,359, Claims 3, 7, 17 U.S. Patent No. RE44,739, Claims 29-32 U.S. Patent No. RE44,654, Claims 14-16 U.S. Patent No. RE44,468, Claims 14, 26, 29, 35, 37, 45 U.S. Patent No. RE46,947, Claims 14, 35, 48, 51, 54, 57 U.S Patent No. 7,676,624, Claim 11</p>	<p>Code representing a PCI bus transaction.</p> <p>PCI bus transaction in serial form.</p>	<p>A PCI bus transaction that has been serialized from a parallel form</p>	<p>“encoded [PCI bus transaction]”: Plain-and-ordinary meaning wherein the plain-and-ordinary meaning is “code representing a PCI bus transaction”</p> <p>“serial”: plain-and-ordinary meaning</p>
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U.S. Patent No. 8,041,873, Claims 54, 77, 97 U.S. Patent No. RE42,984, Claims 40, 52			
<p>#4: “USB”/“Universal Serial Bus (USB) protocol”/“Universal Serial Bus (USB) protocol [data/information]” (proposed by Plaintiff and Defendants)</p> <p>U.S. Patent No. 9,529,768 Claims 33-34, 36, 40 U.S. Patent No. 9,703,750, Claims 4, 7, 24, 46-50 U.S. Patent No. 8,626,977, Claims 1, 4, 11, 17 U.S. Patent No. 8,756,359, Claims 1-8, 17, 19-21 U.S. Patent No. RE44,739, Claims 14, 18-19, 30 U.S. Patent No. RE44,654, Claims 20, 23 U.S. Patent No. RE44,468, Claims 21 U.S. Patent No. RE46,947, Claim 14 U.S. Patent No. 9,529,769, Claim 19</p>	<p>“Universal Serial Bus (USB) protocol” / “Universal Serial Bus (USB) protocol data”: USB data payload “Universal Serial Bus (USB) protocol information”: information described in the USB specification.</p>	<p>[data/information conveyed according to] the protocols defined in the Universal Serial Bus Specification Revision 2.0 and prior versions of the Universal Serial Bus Specification”</p>	<p>Plain-and-ordinary meaning.</p>

<p>#5: “console” (proposed by Plaintiff and Defendants)</p> <p>U.S. Patent No. 9,529,768 Claims 18, 21-22, 30, 34, 40</p> <p>U.S. Patent No. 9,703,750, Claims 5-6, 10-12, 18-20, 24, 35-38, 44-45, 48</p> <p>U.S. Patent No. 8,626,977, Claims 1, 4</p> <p>U.S. Patent No. RE45,140, Claims 14, 17, 31</p> <p>U.S. Patent No. 8,756,359, Claims 1-8, 17, 19-21</p> <p>U.S. Patent No. RE44,739, Claims 18-19</p> <p>U.S. Patent No. RE44,654, Claims 14-16, 20, 23</p> <p>U.S. Patent No. RE43,602, Claim 14</p> <p>U.S. Patent No. 8,041,873, Claims 54, 77</p> <p>U.S. Patent No. RE44,468, Claims 21, 26, 29</p> <p>U.S Patent No. 7,676,624, Claims 6, 11</p> <p>U.S. Patent No. RE42,984, Claims 40, 52</p>	<p>A device or enclosure, housing one or more coupling sites, that connects components of a computer system.</p>	<p>Enclosure, housing at least one bay for receiving a computer module, which connects components of a computer system</p>	<p>A chassis or enclosure, housing one or more coupling sites, that connects components of a computer system.</p>
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<p>#6: “central processing unit (CPU)” (proposed by Defendants)</p> <p>U.S. Patent No. 8,756,359, Claims 1-2, 4, 6, 8, 17, 19; U.S. Patent No. 9,529,768 Claims 1, 4, 7, 10, 13, 18, 22, 30, 33-34, 36, 39; U.S. Patent No. 9,703,750, Claims 1, 5-6, 10-11, 18, 21, 24-25, 27, 29, 31, 34-35, 37-38, 44-48, 50; U.S. Patent No. 8,977,797, Claims 7-8, 10, 14, 16, 36; U.S. Patent No. 8,626,977, Claims 1, 6, 12-14; U.S. Patent No. 9,529,769, Claim 19; U.S. Patent No. RE44,654, Claims 14, 20, 23; U.S. Patent No. RE44,739, Claims 14, 18, 29; U.S. Patent No. RE42,984, Claims 40, 52; U.S. Patent No. RE45,140, Claims 17, 14, 30, 35; U.S. Patent No. RE44,468, Claims 14, 21, 26, 29, 35, 37, 45; U.S. Patent No. RE46,947, Claims 14, 19, 35, 48, 51, 54, 57.</p>	<p>No construction needed. Plain and ordinary meaning.</p>	<p>A core processing unit</p>	<p>Plain-and-ordinary meaning</p>
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U.S. Patent No. RE43,602, Claim 14			
<p>#7: “computer module” (proposed by Defendants)</p> <p>U.S. Patent No. RE43,602, Claims 14; U.S. Patent No. 7,676,624, Claims 11; U.S. Patent No. 8,041,873, Claims 54, 77; U.S. Patent No. RE42,984, Claims 40, 52.</p>	A computing package for providing a computing function as recited in a particular claim.	A user-removable, user- portable computer system within an enclosure comprising at least a processor, memory, and mass storage	A removable computer package

<p>#8: “single chip” (proposed by Defendants)</p> <p>U.S. Patent No. 9,529,768 Claims 1, 4, 13, 18, 22, 36, 39; U.S. Patent No. 9,703,750, Claims 1, 5-6, 10-11, 14, 24- 25, 31, 35, 37, 45, 48, 50; U.S. Patent No. 8,977,797, Claims 36, 38; U.S. Patent No. 8,756,359, Claim 1; U.S. Patent No. 8,626,977, Claims 1, 6, 13-14; U.S. Patent No. 9,529,769, Claim 19; U.S. Patent No. RE44,739, Claims 18, 29; U.S. Patent No. RE43,602, Claim 14; and U.S. Patent No. RE45,140, Claims 14, 30, 35.</p>	<p>No construction needed. Plain and ordinary meaning.</p>	<p>One integrated circuit chip</p>	<p>Plain and ordinary meaning</p>
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